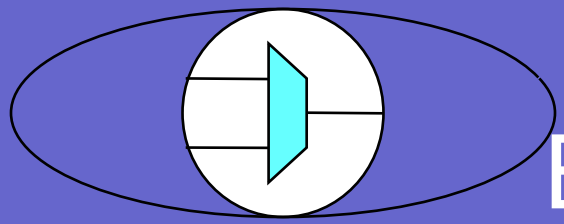
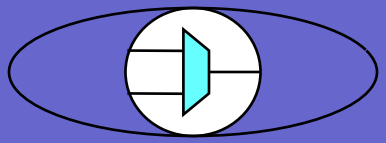


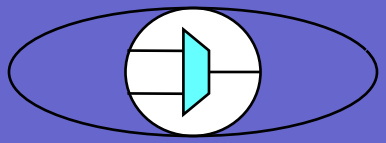
HDL Dynamics®
Enabling SoC Solutions

Overview and Strategies



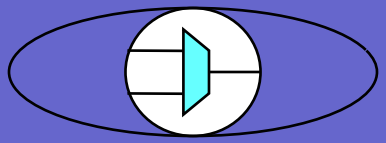
Background

- HDL Dynamics was originally chartered in 2000 as an IP and tools development consulting and business vehicle.
- Principal Engineer is Neal Stollon
- Re-focused in 2007 to address opportunities in emerging areas in SoC and multicore infrastructure and development
  - Debug and In Silicon Instrumentation IP
  - Performance analysis based optimization
  - Tools and interfaces tying together disconnects between ESL (Electronic System Level) and On-Chip Analysis



About Neal Stollon

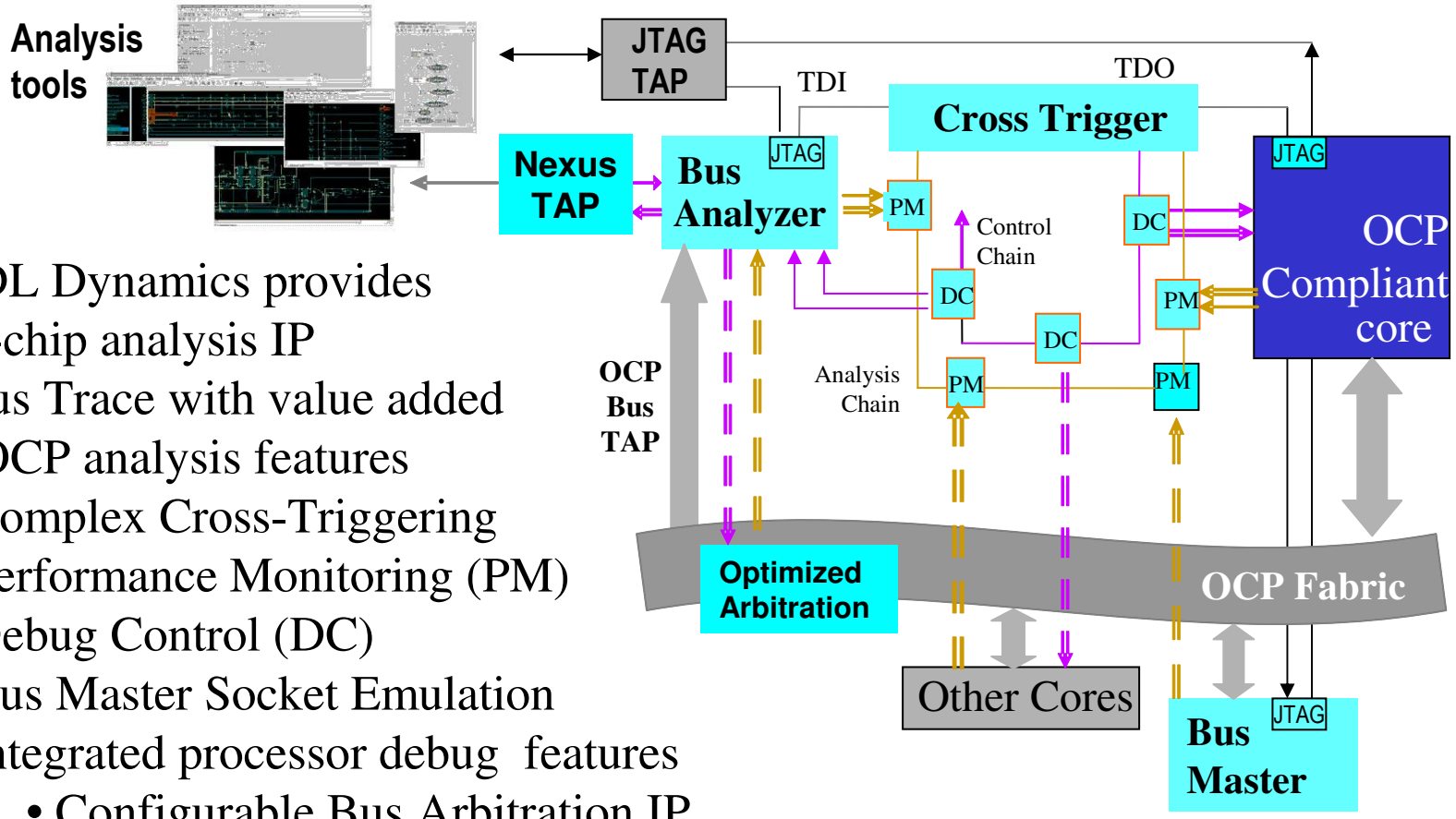
- 20+ years industry work in digital systems and IP, processor and networking architectures and infrastructure, EDA (RTL/ESL) tools development
- Strong Technical focus
  - **PH.D in EE from Southern Methodist University**
  - **Professional Engineer (Texas)**
  - **10 patents awarded or in work**
  - **35 published technical papers and articles**
- Strong Business and Program Management Focus
  - **Large company experience (TI, Alcatel, LSI Logic, MIPS)**
  - **Small company experience (Infinite Technology, FS2)**
- Focus areas
  - **On Chip Debug technologies**
  - **Digital IP Development and Technical Marketing**



Addressing Industry Challenges

- Multicore SoC Development is emerging trend
  - Tools and IP TAM $500M -$5B
  - Projected to increase >4x over next 5 years
  - Industry flows have many holes and missing pieces
  - Better SoC infrastructure is a emerging business opportunity
- Multicore SoC analysis and verification is challenging
  - **No integrated flows from ESL to RTL to final silicon**
  - **Multicore analysis requires new analysis and optimization tools**
  - **Reuse from one analysis level to another is limited (but required)**
- Instrumentation based Debug analysis is critical
  - **Limited other means to access required on-chip data**
  - **Few options for integrated, vender neutral solutions**
- **HDL Dynamics has expertise and resources in this space**

System Debug Instrumentation OCP Example

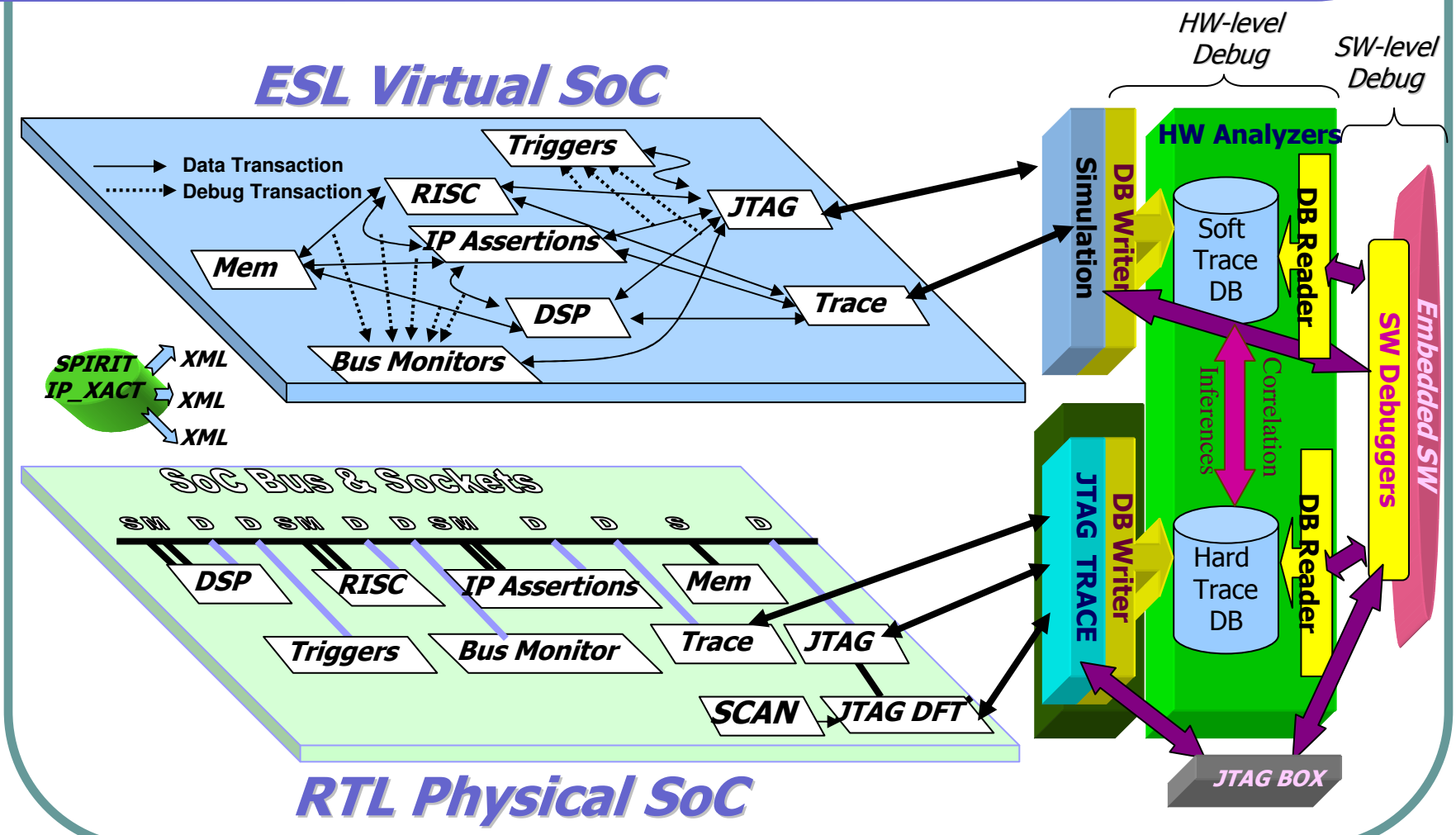


HDL Dynamics provides on-chip analysis IP

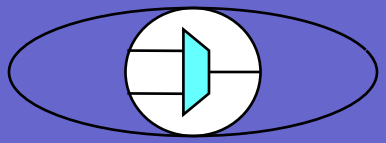
- Bus Trace with value added OCP analysis features
- Complex Cross-Triggering
- Performance Monitoring (PM)
- Debug Control (DC)
- Bus Master Socket Emulation
- Integrated processor debug features
  - Configurable Bus Arbitration IP

Compatible with JTAG 3rd party instruments and tools

Next Stage Debug Challenges: Integrating ESL and Debug



HDL Dynamics
SoC Solutions



Areas of 2007 Focus

- Development of Instrumentation and Analysis tool suite
  - Focus on Performance Analysis based debug instrumentation
  - Integrating debug IP flow to better support ESL and RTL tools
  - Develop on-chip instrumentation based optimization technologies
  - Developing standards based solutions (ex. Nexus, OCP, AMBA)
- Developing industry partnerships and relationships
  - Product co-development – fielding and marketing initial solutions
  - Access to complementary solutions
- Pursuing seed funding and investment
  - **Seed money through consulting/ product development engagements**
  - **DoD SBIRs submitted on multicore optimization and debug**
  - **Longer term investment capital**